DDR5-6000	fallback	"easy"	BZ lazy			
UCLK to MCLK	1:1	1:1	1:1			
MCLK	3000	3000	3000			
UCLK	3000	3000	3000			
FCLK	2000	2000	2133			
VSOC	1.25	1.25	1.25			
DRAM VDD	1.35	auto	1.43			
DRAM VDDQ	auto	auto	auto			
VDDIO	auto	auto	auto			
VDDP	0.95	0.95	0.95			
tCL	32	XMP/EXPO	30			
tRCDWR	38	XMP/EXPO	16	**if your motherboard doesn't have tRCDWR only use tRCDRD**		
tRCDRD	38	XMP/EXPO	36			
tRP	38	XMP/EXPO	36			
tRAS	126	126	126			
tRC	60	60	60			
tWR	48	48	48			
tRFC	512	512	512			
tRFC2	not used	not used	not used			
tRFCSB	not used	not used	not used			
tREFI	40000	50000	65535	RAM fan recommended for 65535		
tRTP	16	16	16			
tRRDL	8	8	8			
tRRDS	8	8	4			
tFAW	32	32	20			
tWTRL	16	16	16			
tWTRS	6	4	4			
tRDRDSCL	4	4	4			
tRDRDSC	1	1	1			
tRDRDSD	6	6	6	this timing only applies to multi rank setups		
tRDRDDD	6	6	6	this timing only applies to multi rank setups		
tWRWRSCL	4	2	2			
tWRWRSC	1	1	1			
tWRWRSD	8	8	8	this timing only applies to multi rank setups		
tWRWRDD	8	8	8	this timing only applies to multi rank setups		
tWRRD	4	4	4			
tRDWR	16	16	16			
Nitro RX Data	auto	auto	1			
Nitro TX Data	auto	auto	2			
Nitro Control Line	auto	auto	0			

DDR5-6200	fallback	"easy"	BZ lazy	WARNING!	
				the UMC on some very unlucky Ryzen 9000 CPUs simply will not do 3100MHz even at 1.3VSOC which makes DDR5-6200 1:1 impossible. You'll want to run 1:1 6000 or 2:1 7600+	
UCLK to MCLK	1:1	1:1	1:1		
MCLK	3100	3100	3100		
UCLK	3100	3100	3100		
FCLK	2066	2066	2066	if you can get it stable 2166 or 2200 FLCK is a bit faster	
VSOC	1.3	1.3	1.3		
DRAM VDD	1.35	auto	1.43		
DRAM VDDQ	auto	auto	auto		
VDDIO	auto	auto	auto		
VDDP	0.95	0.95	0.95		
tCL	34	XMP/EXPO	32		
tRCDWR	40	XMP/EXPO	16	**if your motherboard doesn't have tRCDWR only use tRCDRD**	
tRCDRD	40	XMP/EXPO	37		
tRP	40	XMP/EXPO	37		
tRAS	126	126	126		
tRC	62	62	62		
tWR	48	48	48		
tRFC	544	512	512		
tRFC2	not used	not used	not used		
tRFCSB	not used	not used	not used		
tREFI	40000	50000	65535	RAM fan recommended for 65535	
tRTP	16	16	16		
tRRDL	8	8	8		
tRRDS	8	8	4		
tFAW	32	32	20		
tWTRL	16	16	16		
tWTRS	6	4	4		
tRDRDSCL	6	4	4		
tRDRDSC	1	1	1		
tRDRDSD	6	6	6	this timing only applies to multi rank setups	
tRDRDDD	6	6	6	this timing only applies to multi rank setups	
tWRWRSCL	6	2	2		
tWRWRSC	1	1	1		
tWRWRSD	8	8	8	this timing only applies to multi rank setups	
tWRWRDD	8	8	8	this timing only applies to multi rank setups	
tWRRD	6	4	4		
tRDWR	18	16	16		
Nitro RX Data	auto	1	1		
Nitro TX Data	auto	3	2		
Nitro Control Line	auto	1	0		

DDR5-6400	fallback	"easy"	BZ lazy	WARNING!	
				the UMC on many Ryzen 9000 CPUs simply will not do 3200MHz even at 1.3VSOC which makes DDR5-6400 1:1 impossible. You'll want to run 1:1 6200 or 2:1 7600+	
UCLK to MCLK	1:1	1:1	1:1		
MCLK	3200	3200	3200		
UCLK	3200	3200	3200		
FCLK	2100	2133	2133		
VSOC	1.3	1.3	1.3		
DRAM VDD	1.35	auto	1.43		
DRAM VDDQ	auto	auto	auto		
VDDIO	auto	auto	auto		
VDDP	0.95	0.95	0.95		
tCL	34	XMP/EXPO	32		
tRCDWR	40	XMP/EXPO	16	**if your motherboard doesn't have tRCDWR only use tRCDRD**	
tRCDRD	40	XMP/EXPO	38		
tRP	40	XMP/EXPO	38		
tRAS	126	126	126		
tRC	64	64	64		
tWR	48	48	48		
tRFC	544	544	544		
tRFC2	not used	not used	not used		
tRFCSB	not used	not used	not used		
tREFI	40000	50000	65535	RAM fan recommended for 65535	
tRTP	16	16	16		
tRRDL	10	8	8		
tRRDS	8	8	4		
tFAW	32	32	20		
tWTRL	16	16	16		
tWTRS	6	4	4		
tRDRDSCL	6	6	4		
tRDRDSC	1	1	1		
tRDRDSD	6	6	6	this timing only applies to multi rank setups	
tRDRDDD	6	6	6	this timing only applies to multi rank setups	
tWRWRSCL	6	2	2		
tWRWRSC	1	1	1		
tWRWRSD	8	8	8	this timing only applies to multi rank setups	
tWRWRDD	8	8	8	this timing only applies to multi rank setups	
tWRRD	6	4	4		
tRDWR	18	16	16		
Nitro RX Data	auto	auto	1		
Nitro TX Data	auto	auto	3		
Nitro Control Line	auto	auto	1		

fallback	this is mainly meant as a starting point for kits that really don't want to work at the better settings		
"easy"	settings I would expect to work basically always		
BZ lazy	what I'd probably try with my daily system		
MCLK to UCLK	ratio of DRAM + PHY clock to memory controller clock		
UCLK	memory controller clock	less latency + more bandwidth	
MCLK	DRAM + PHY clock	less latency + more bandwidth	
FCLK	infinity fabric clock	less latency + more bandwidth	
VSOC	SOC voltage	0.9-1.3V max	primarily affects your max UCLK. in 2:1 mode the low UCLK allows some very low SOC voltages
DRAM VDD	DRAM "core" voltage	1.35-1.75V	high VDD(1.5V+) is maily about running low tCL (like 8000C34 or 6400C26). More than 1.65V can cause worse stability
DRAM VDDQ	DRAM IO voltage RAM to CPU signaling	1.1-1.65	I wouldn't go over 1.65V. Optimal value varies by motherboard + RAM + BIOS version. usually between 1.25 and 1.45V
VDDIO	PHY IO voltage CPU to RAM signaling	1.1-1.5V	1.5V max. Optimal value varies by motherboard + RAM + BIOS version. usually between 1.25 and 1.5V
VDDP	PHY voltage	0.95-1.15V	1.15V max. If you set this too low or too high the system won't be stable.
tCL	READ command to data burst output	reduces read and write latency	
tRCDWR	ACT to WRITE command delay. How long you wait for a row to open before sending a WRITE	reduces write latency	can be very short because we are writing over the data in the row.
tRCDRD	ACT to READ command delay. How long you wait for a row to open before sending a READ	reduces read latency	
tRP	PRE to ACT in same bank delay. How soon you try to open a different row in the bank.	faster row change	
tRAS	ACT to PRE in same bank delay. How soon after opening a row you try to close it.	row hoping	only relevant if the MC opens a row and then "immediately" wants to close it
tRC	ACT to ACT in same bank delay. How quickly you can change active rows.	row hoping	only relevant if the MC opens a row and then "immediately" wants to open a different one
tWR	WRITE to PRE in same bank delay. How soon you try to close a row after sending a WRITE	faster row change	
tRFC	REFRESH duration. How long you wait after a REF command before sending any other commands	more "usable" clock cycles	tRFC / tREFI = fraction of clock cycles "wasted" on refresh
tRFC2	unused		
tRFCSB	unused		
tREFI	REFRESH interval. How long you wait between REF commands	more "usable" clock cycles	DRAM data retention gets worse with temperature. High tREFI values require low temps. usually less than 55C for 65000
tRTP	READ to PRE. How soon after a READ you try to close a row	faster row change	
tRRDL	ACT to ACT same bank group. How long you wait before trying to active a row in a different bank of the group	faster row change	setting these bellow 8 doesn't do much since DDR5's bust length is 8 cycles
tRRDS	ACT to ACT different bank group. How long you wait before trying to active a row in any bank of a different group	faster row change	setting these bellow 8 doesn't do much since DDR5's bust length is 8 cycles
tFAW	Four ACT Window. Delays a 5th ACT command if 4 ACT commands happened too quickly	faster row change	
tWTRL	WRITE to READ same bank group. How soon you try to READ from the same bank group after a WRITE burst	more memory bandwidth	
tWTRS	WRITE to READ different bank group. How soon you try to READ from a different bank group after a WRITE burst	more memory bandwidth	
tRDRDSCL	READ to READ same bank group.	more memory bandwidth	
tRDRDSC	READ to READ different bank group.	more memory bandwidth	anything more than 1 is a disaster for memory bandwidth
tRDRDSD	READ to READ different rank same DIMM	more memory bandwidth	
tRDRDDD	READ to READ different rank different DIMM	more memory bandwidth	
tWRWRSCL	WRITE to WRITE same bank group.	more memory bandwidth	
tWRWRSC	WRITE to WRITE different bank group.	more memory bandwidth	anything more than 1 is a disaster for memory bandwidth
tWRWRSD	WRITE to WRITE different rank same DIMM	more memory bandwidth	
tWRWRDD	WRITE to WRITE different rank different DIMM	more memory bandwidth	
tWRRD	WRITE to READ different ranks?	more memory bandwidth	
tRDWR	READ to WRITE any scenario	more memory bandwidth	